**25th International Conference on Electronic Packaging Technology**
**August 07 to 09, 2024, Tianjin, China**
**http://www.icept.org**

**Speech subject：** Predictive Design and Modeling on Fan-Out Technology

***Speech leader:*** CHE Faxing—Senior Member of Technical Staff, Micron Semiconductor Asia Operations Pte. Ltd

**Speech Description/Objective:**

Fan-out packaging (FOP) technology has gained prominence and more and more application in advanced electronic packaging due to its ability to address the challenges for high density, high-performance, high-speed requirement by high integrated IC packages. However, it also faces additional challenges such as wafer/panel level warpage, die shift, reliability issues. This speech will cover FOP technology evolution history, advantages, FO wafer-level /FO panel-level packaging process, trend and application, challenges from technical point view. RDL-first and mold-first FOP will be discussed and compared.

SMART (Structure-Material-Assembly-Reliability-Thermal) co-design simulation methodology will be introduced to solve technical challenges and provide optimal solution for FOP technology systematically. Three case studies will be presented to understand how numerical simulation helps to overcome technical issue and optimize design and process for FOP technology. First case relating to TSV-free interposer (TFI) using FOWLP technology includes co-design modeling for wafer warpage, package warpage, package and board level reliability, and thermal performance. Second case regarding FOPLP using RDL first approach focus on process dependent panel warpage. Taguchi method is used to investigate factor significance and optimize design and reliability. Third case talking about panel warpage and die shift for FOPLP with mold first approach. The effect of weight on panel warpage is investigated and interesting results are discussed. Large thin panel may result in less warpage compared to small panel with considering weight effect, which is consistent with experimental observation. New methodology on die shift simulation and calculation is proposed for FOPLP technology with large panel of 650mm x 550mm size.

**Speech Outline:**

1. Introduction on FOWLP/PLP (Fan-out wafer-level packaging / panel-level packaging)
- What/When/Why/Who/How
- Trend, Opportunities/Application, Challenges

2. Modeling and Simulation on FOWLP/PLP
- Co-design Simulation Methodology (SMART)
- Case Study (warpage, die shift, solder joint reliability)
  - ✧ TSV-Free Interposer (TFI) with FOWLP
  - ✧ FOPLP – RDL first approach
  - ✧ FOPLP – mold first approach

3. Summary & Key Take Away (Q/A)

**Who Should Attend:**

Engineers, managers from Semiconductor advanced packaging related industry covering packaging and assembly process, materials, reliability, design, modeling and simulation, especially in fan-out packaging technology including wafer level and panel level packaging warpage control and optimization.

Students and professionals in advanced packaging modeling and simulation area, material characterization and package design area.

**Introduction of Speaker:**

**Faxing Che** received the **Ph.D. degree** in Engineering Mechanics from Nanyang Technological University, Singapore, in 2006.

He is a **Senior Member of Technical Staff** with Micron Semiconductor Asia Operations since 2020. Dr. Che has more than **20 years' experience** in advanced microelectronic packaging technologies in top industrial and academic organizations. He worked with United Test and Assembly Center Ltd (UTAC) and STMicroelectronics, Singapore. Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR) and Infineon Technologies Asia Pacific.

Dr. Che was a recipient of **4 Best International Conference Paper Awards** (EPTC2003, EPTC2013, Itherm2006, ICEPT2006).

He has co-authored **one book** and over **170 technical papers** in refereed journals and conference proceedings in advanced microelectronics packaging area. He has **11 US patents** granted or in application.

His **research interests** include design for reliability in advanced packaging, Cu wire bonding, through silicon via (TSV) technology, fan-out wafer-level/panel-level packaging, finite-element modeling and simulation, characterization of microelectronic packaging materials, physic driven and data driven machine learning approach for express technical risk assessment of advanced packaging technology.

Dr. Che serves as a **Peer Reviewer** for more than 35 international scientific journals such as J. of Materials Science, J. of Electronic Materials, J. Materials and Design, Materials characterization, Microelectronics Reliability, IEEE Trans. on CPMT, IEEE Trans. on DMR, International J. of Fatigue, J. of Alloys and Compounds, J. of Micromechanics and Microengineering, etc.

Dr. Che is named in World's **Top 2% Scientists** in 4 consecutive years from 2020 to 2023 by Stanford University.

He is an IEEE **senior member**.

-