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<http://www.icept.org>

Speech subject: Design and Process Considerations for 2.5 Interposer Technology.

Speech leader: Gu-Sung Kim, Professor, Kangnam University

Speech Description/Objective:

Modern Semiconductor technology is a position representing competitiveness among countries. Due to the preoccupation of semiconductor front-end technology by a few countries, most of the countries that were left out of ranks are strengthening support for semiconductor back-end technology, such as China, Japan, Southern Asia, and Europe.

Unlike the eight major semiconductor processes, it is difficult to understand the flow of the entire technology in the semiconductor middle-end process due to its diversity and variability. Heterogeneous Integration is new era technology, integration of separately manufactured into a higher-level assembly that provides functional improvements.

The Presenter explains the semiconductor Middle-End Process and its Technology, with 3 types of TSVs(Through Si Via) from the assembly technology mentioned in the ITRS last version to the Heterogeneous Integration technology in the IEEE EPS HIR. In addition, present what is considerable design and process concepts including electrical, mechanical, and thermal simulations in this area.

Introduction of Speaker:

Gu-Sung Kim, Ph.D., Th.M. is currently a faculty position at Kangnam University and a founder of EPRC (Electronics Packaging Research Center). He had 35 years experiments for R&D of Semiconductor Packaging. Prior to joining and establishing lecture/research position, Kim was a 3D IC/TSV/WLP project leader for Samsung Electronics Co., Ltd, IPT team, Memory Division for 17 years. He has more 130 Patents as an inventor in Korea and USA related 3D IC, TSV, and Interposer. He published 2 semiconductor packaging handbooks and presented more 100 as a speaker and talk. He received several awards from Korea government, Society, Samsung, KSIA, SEMI, and Alfred Marquis Lifetime etc.

Kim received a Ph.D. degree in materials engineering from Rensselaer Polytechnic Institute, Troy, NY, USA., a BS degree in ceramic engineering from Yonsei University, Seoul, Korea.

Currently, He serve a member of post Board-of-Governors (BoG) of IEEE EPS (eps.ieee.org), chair of IEEE EPS Korea Chapter (EP21, www.ieee-epskorea.org). vice-chair of KSDT (Korea Semiconductor Display Technology Society), deputy-chair of EPRC, and Technical Director at KMEPS (Korea Microelectronics and Packaging Society). He also has a position of chair of board at Electro-Package Mission Society (www.epcross.org), technical committee of Korea industrial technology security agency, SEMI STS, and Semiconductor Korea Symposium.