Speech subject： DTCO for warpage & thermal control in wafer level advanced packaging.

Speech leader: Xin WANG ——CTO, VP of R&D, Hangzhou Microsilicon Technology Co.,Ltd

Speech Description/Objective:

As the semiconductor chips' fabrication keeps moving towards the direction of miniaturization and function increment which means more I/Os or interconnection pads on the same area of chip, in terms of the chips' packaging, the industry has been adopting more and more wafer level advanced packaging technology. Among all the WLP (Wafer Level Packaging) types, FOWLP (Fan Out WLP) is the one which has more flexible packaging architecture and cost performance trade-off, thus has relatively faster market growth in recent years.

Wafer warpage and thermal management are the two critical challenges for almost all types of the advanced package. This report will share some of the learning and experience on those two topics in FOWLP (Fan Out Wafer Level Package), on the basis of theoretic modeling & analysis, also the experimental data, to show the importance of DTCO (Design Technology Co-Optimization) for warpage and thermal management, e.g., package architecture design such as thickness and area ratio, material property, process flow, etc. Those kind of systematic study could help providing the optimal packaging solutions for different customers' product requirement.

Who Should Attend:

fabless, package house, module or material suppliers,

Introduction of Speaker:

Xin WANG is currently the CTO and VP of R&D at Hangzhou MicroSilicon Technology Co.,Ltd, since he returned back to China from Singapore and co-founded the company in 2018.

Previously, he held position as senior R&D manager in Singapore Advanced Package Development Center at Applied Materials Inc., during the over 10+ years in Applied advanced package group, he was focusing on the process material integration and equipment development related to various wafer-level advanced packaging solutions (including face down & face up FOWLP, 2.5D/3D FOSiP, TSV, etc.), his main serviced customers and project collaboration partners include Apple, TSMC, Intel, SPIL and etc.

After joined in MicroSilicon Technology Co.,Ltd, he has been responsible for building up the core R&D and engineering team for packaging design、 simulation、 process integration and new product penetration, also setting up the first advanced wafer level production line for the company (already started mass production since 2023). His strong expertise is mainly on wafer level package, SiP, 2.5D/3D advanced package and chiplet integration.

Xin WANG received his Master degree from Xi'an Jiaotong University, and holds more than 30+US/China patents.