Speech subject： “Manufacturing Technology Solution of Wafer / Panel Level Packaging for Chiplet Integration”

Speech leader: motoshi kobayashi—General Manager,ULVAC, Inc.

Speech Description/Objective:
The next era of AI-driven information and communications technology (ICT) systems will be powered by an infrastructure that integrates Cloud Computing, Fog and Edge Computing, and Massive IoT. New semiconductor devices are necessary for artificial intelligence (AI) that require real-time or low-latency performance (less than 1ms), as well as low power consumption. High-density packaging technologies, including 3D chiplet integration with wafer-level packaging (WLP) and panel-level packaging (PLP), are essential to meet the manufacturing requirements of these high-performance semiconductor devices. ULVAC has been continuously developing manufacturing solutions to achieve heterogeneous integration through substrate packaging, 2.5D interposers, and 3D-IC technologies, including through-silicon vias (TSV) and hybrid bonding. In this presentation, ULVAC will outline our efforts in heterogeneous chiplet integration, which involve plasma etching/ashing and PVD (Physical Vapor Deposition) sputtering techniques to achieve high-density interconnections.

Speech Outline:
1. Introduction & Background
2. Manufacturing Technology Transformation by Chiplet Integration
3. Dry process development strategy for Chiplet Integration
    3-1. Wafer Level Process for FO-RDL, TSV etch and Plasma dicing
    3-2. Panel Level Process for Build up and FO-RDL interposer
4. Collaborative activities
5. Summary

Introduction of Speaker:

Motoshi Kobayashi is the General Manager of the Institute of Advanced Technology at ULVAC Inc. and is responsible for the key technologies of vacuum equipment for semiconductors, electric devices, and flat panel production. He is also the Chairman of the ULVAC Research Center of Suzhou.

He has been working for over 20 years at ULVAC in the development of technologies for sputtering processes and targets for semiconductors, electric devices, and flat panel displays. In particular, he has developed sputtering processes and targets for oxide metal TFTs and contributed to their widespread adoption in industry. He is leading the overall development of new manufacturing equipment in the institute. Currently, focuses on dry-etching and sputtering technologies for advanced packaging. He graduated with a degree in physics from the Graduate School of Science and Engineering, Shizuoka University (Japan), and was granted the degree of Master of Science in 2003.