25th International Conference on Electronic Packaging Technology

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Course subject：

Chiplet Design and Heterogeneous Integration Packaging

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Speech Description/Objective:

Chiplet is a chip design method and heterogeneous integration is a chip packaging method. Chiplet design and heterogeneous integration packaging have been generated lots of tractions lately. For the next few years, we will see more implementations of a higher level of chiplet designs and heterogeneous integration packaging, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the following topics will be covered.

- System-on-Chip (SoC)
- Why Chiplet Design?
- Chiplet Design and Heterogeneous Integration Packaging – Chip Partition and Chip Split
  (1) Chip partition and Heterogeneous Integration
  (2) Chip split and Heterogeneous Integration
  (3) Advantages and Disadvantages
- Communication between Chiplets (e.g., Bridges)
  Bridge Embedded in Build-up Package Substrate
  Bridge Embedded in Fan-Out EMC with RDLs
  UCIe
  Hybrid Bonding Bridge
- Chiplet Design and Heterogeneous Integration Packaging - Multiple System and Heterogeneous Integration
  (1) Multiple System and Heterogeneous Integration with Package Substrate (2D IC Integration)
  (2) Multiple System and Heterogeneous Integration with Thin Film layer on the Package Substrate (2.1D IC Integration)
  (3) Multiple System and Heterogeneous Integration with TSV-less (Organic) Interposer (2.3D IC Integration)
  (4) Multiple System and Heterogeneous Integration with Passive TSV-Interposer (2.5D IC Integration)
  (5) Multiple System and Heterogeneous Integration with Active TSV-Interposer (3D IC Integration)
- Advanced Packaging Driving by Artificial Intelligent
- Glass Core Substrates
- Summary
- Potential R&D Topics in Chiplet Design and Heterogeneous Integration Packaging

- Trends in Chiplet Design and Heterogeneous Integration Packaging

Who Should Attend:
If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. The lectures are based on the publications by many distinguish authors and the books by the lecturer.

Introduction of Speaker：
John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 520 peer-reviewed papers (375 are the principal investigator), 52 issued and pending US patents (30 are the principal inventor), and 23 textbooks (all are the first author), e.g., Chiplet Design and Heterogeneous Integration Packaging (525 pages, Springer, 2023). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.