



**Course subject:**

**"Less is Moore" for Chiplets and Glass Substrates**

*Course leader: Wei Koh, PhD*

**Course Description:**

Chiplet packaging technology is being hotly pursued by the semiconductor and backend OSAT industry. In China, it is further deemed as a savior and opportunity to “Passing at the Bending Racetrack,” since we are behind in making advanced node System-on-Chip (SoC).” In “More than Moore”, heterogeneous integration (HI) and high-density glass substrates are the two key enabling solutions for chiplet packaging. This course will provide a detailed review of the progress in chiplet technology, heterogeneous Integration methodologies, and development in TGV glass interposers and substrates. As heterogeneous integration is becoming more complex and more difficult, we need to further improve HI with innovations to convert “More than Moore” to “Less is Moore”—meaning, less complex designs and standards, less power consumption packages, and less manufacturing cost.

The main topics covered include:

1. Chiplet concept evolution and benefits
2. Chiplet technical challenges and open ecosystem requirements
3. Homogeneous Integration versus Heterogeneous Integration
4. The five “I’s” of chiplet heterogeneous integration:
  - Interface—heterogeneous die-to-die (D2D) interface characterization
  - Interoperability—compatibility among different IP chiplets, different nodes/processes, different manufacturers, different form factors
  - Interconnection—methods and standards, data rate
  - Interaction—chip package interaction (CPI), D2D interactions
  - Interchange—ability to change or replace diverse chiplet components
5. TGV glass interposer and substrate technology development
6. “Less is Moore” innovations and open ecosystem requirements

**Introduction of Speaker:**

Dr Koh has been working on IC packaging and microelectronics assembly technologies since the early 1980’ s. He has MS and PhD degrees from Cornell University and worked for Henkel, Motorola, and Kingston Technology. As a Fellow of IEEE EPS, he has over 90 publications and 40 US patents relating to microelectronics.